REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, the subject matter of claim 7 has been incorporated into each of claims 1, 18, 19, 20 and 21; in light thereof, claim 7 has been cancelled without prejudice or disclaimer. These claims, 1, 18, 19, 20 and 21 have been further amended to recite that the silicon nitride insulating film is deposited "over" the semiconductor substrate, and that the silicon oxide insulating film is deposited "over" the silicon nitride insulating film. Moreover, in light of amendments to claims 1, claim 8 has been amended to recite "the" temperature of the semiconductor substrate being plasma etched; and in light of antecedent basis requirements, claim 13 has been amended to recite "a" flow rate of the argon gas.

Moreover, each of claims 22, 37, 38, 39 and 40 has been amended to recite that the silicon oxide insulating film is deposited "over a patterned silicon nitride film with a silicon plug over" a semiconductor substrate; to recite that the hard mask is formed "over" the silicon oxide insulating film; and to recite that the semiconductor substrate is subjected to a plasma etching treatment through the hard mask using a specified etching gas "so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the silicon plug is exposed". Note, for example, and not to be limiting, the paragraph bridging pages 66 and 67 of Applicants' specification, together with Fig. 42.

The objection to claim 13 as set forth in Item 1 on page 2 of the Office Action mailed January 13, 2003, is noted. Applicants have followed the suggestion by the Examiner to overcome this objection; accordingly, this objection is clearly moot.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the reference applied by the Examiner in rejecting claims in the Office Action mailed January 13, 2003, that is, the teachings of U.S. Patent No. 6,159,862 to Yamada, et al, under the provisions of 35 USC 103.

Initially, Applicants note reference by the Examiner to the U.S. Patents to Liu, et al, No. 6,403,491, to Collins, et al, No. 6,238,588, to Jeng, et al, No. 5,282,925, and to Toprac, et al, No. 6,238,937, in the sole full paragraph on page 3 of the Office Action mailed January 13, 2003. While the Examiner apparently relies on these U.S. Patents has evidence for establishing obviousness of the presently claimed subject matter, the Examiner has not used any of these references in the formal statement of the rejection, has not indicated combinability of the teachings of these references with the teachings of Yamada, et al, and has not indicated any motivation to combine teachings of the references. Clearly, reliance by the Examiner on the teachings of these U.S. Patents listed in the sole full paragraph on page 3 of the Office Action mailed January 13, 2003 is improper. See In re Hoch, 166 USPQ 406, 407n.3 (CCPA 1970).

If the Examiner intends to rely on the teachings of any reference, of these references listed in the sole full paragraph on page 3 of the Office Action mailed January 13, 2003, other than the teachings of Yamada, et al, it is respectfully submitted that the Examiner must incorporate such reference in the formal statement of the rejection, and satisfy requirements of 35 USC 103 in connection with combining teachings of references.

In any event, the undersigned notes the date, for prior art purposes, of U.S.

Patent No. 6,403,491 to Liu, et al (that is, November 1, 2000). This date of November 1, 2000 is after the filing date of the Japanese Priority Application (No. 2000-200986, filed July 3, 2000) of the above-identified application, which is being relied upon under 35 USC 119 herein. A claim for priority based on No. 2000-200986, under 35 USC 119, was made in the Declaration under 37 CFR 1.63 filed in the above-identified application, as well as in a Letter Claiming Right Of Priority filed June 29, 2001; and a certified copy of the Japanese Priority Application has already been filed. The Examiner has acknowledged the claim for foreign priority as well as receipt of the priority document, in the Office Action Summary of the Office Action mailed January 13, 2003.

For completing requirements of 35 USC 119 and 37 CFR 1.55, enclosed please find an English translation of No. 2000-200986, together with a Declaration of accuracy of the translation. Thus, it is respectfully submitted that all procedural requirements of 35 USC 119 and 37 CFR 1.55 have been satisfied, for applicants' to be accorded benefit of the filing date of No. 2000-200986.

Moreover, as can be seen in the enclosed English translation, No. 2000-200986 is directed to the same invention, and fully supports the presently claimed subject matter within the meaning of the first paragraph of 35 USC 112. Note, for example, pages 14 - 24 and 74 – 76 of the enclosed English translation.

In view of the foregoing, it is respectfully submitted that, at the least, U.S. Patent No. 6,403,491 does not constitute prior art in connection with the subject matter claimed in the above-identified application.

It is respectfully submitted that the reference as applied by the Examiner would have neither taught nor would have suggested a fabrication method of a semiconductor

integrated circuit device, as in the present claims, including depositing the various layers and performing a plasma etching treatment, wherein the residence time of the etching gas within the etching chamber is set at 50 - 700 ms, and the temperature of the semiconductor substrate being plasma etched ranges from 60 to 140°C. See claim 1; note also, claims 18 and 19, defining more specific ranges for the residence time of the etching gas within the etching chamber. See also claims 20 and 21, defining the temperature of the substrate being plasma-etched, and also reciting that a pressure within the etching chamber during the plasma etching treatment ranges from 0.7 to 7 Pa and a total flow rate of the etching gas passed into the etching chamber is 700 cm^3/minute (see claim 20), or reciting that a pressure within the etching chamber during the plasma etching ranges from 1.3 to 4 Pa and a total flow rate of the etching gas passed into the etching chamber is 700 cm^3/minute or over (see claim 21).

Moreover, it is respectfully submitted that the applied reference would have neither taught nor would have suggested other aspects of the present invention, having the features as in claim 1, and additionally, the pressure within the etching chamber as in claim 2, or total flow rate of the etching gas passed into the etching chamber as in claims 3 and 4, or both pressure within the etching chamber and total flow rate of the etching gas as in claim 5; and/or wherein a flow rate of the dilution gas is larger than the flow rates of the fluorocarbon gas and oxygen (see claim 6); and/or more specific temperature of the semiconductor substrate being plasma etched as in claim 8; and/or plasma density during the plasma etching, as in claims 9 and 10; and/or specific materials for the fluorocarbon gas and dilution gas as in claim 11, with flow rate of the dilution gas as in claims 12 and 13 and ratio of flow rates as in claims 14 and 15; and/or

partial pressure of the fluorocarbon gas as in claims 16 and 17.

Furthermore, it is respectfully submitted that the teachings of Yamada, et al, would have neither disclosed nor would have suggested such a semiconductor integrated circuit fabrication method as in the present claims, including the processing wherein a silicon oxide insulating film is deposited over a patterned silicon nitride film with a silicon plug over a semiconductor substrate, and after forming a hard mask over the silicon oxide insulating film, the substrate is subjected to a plasma etching treatment through the hard mask using a specified etching gas including a fluorocarbon gas so as to form a hole in the silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the silicon plug is exposed. See claim 22; note also claims 37, 38, 39 and 40.

Moreover, it is respectfully submitted that the teachings of Yamada, et al would have neither disclosed nor would have suggested the other aspects of the present invention as in claims ultimately dependent on claim 22, having the features as set forth in claim 22, and further having a pressure within the chamber during plasma etching which ranges from 0.7 to 7 Pa (see claim 23), or wherein a total flow rate of the etching gas passed into the etching chamber is that set forth in claims 24 and 25, or wherein the pressure within the etching chamber and the total flow rate of the etching gas is that set forth in claim 26; and/or wherein the flow rate of the dilution gas is larger than the flow rates of the fluorocarbon gas and oxygen (see claim 27); and/or plasma density during the plasma etching as in claims 28 and 29; and/or wherein the fluorocarbon gas is made of C_5F_8, with the dilution gas being made of argon (see claim 30), with flow rates of the argon gas as in claims 31 and 32, and a ratio in flow rate between the oxygen and C_5F_8

as in claims 33 and 34; and/or partial pressure of C_5F_8 as in claims 35 and 36.

The present invention is directed to a method of fabricating a semiconductor integrated circuit device, particularly effective in a process forming a self-aligned contact (SAC) or a high aspect ratio contact (HARC) in fabricating semiconductor integrated circuit devices.

As described on page 1 of Applicants' specification, there has been disclosed a technique wherein a silicon oxide layer is etched while ensuring great selectivity to a silicon nitride layer, using perfluorocycloolefins (containing C_5F_8) as an etching gas.

However, as a tendency toward a high aspect ratio increases as the design rule of integrated circuit manufacture is scaled down, it is necessary to improve an ease-in-etching property and also improve selectivity ratio of etching silicon oxide to silicon nitride. However, as described on page 3 of Applicants' specification, in the techniques of the SAC process and HARC process, where the aspect ratio (depth/width) of a hole or groove is increased, Applicants have found that there arises a problem in improving both the ease-in-etching property and etching selectivity of silicon oxide to silicon nitride. For example, where etching is carried out to enhance the ease-in-etching property of the silicon oxide film, to make a hole or groove, the selectivity ratio between the silicon oxide film and the silicon nitride film can not be ensured, so that a margin for short-circuiting between a conductor film buried in a hole or groove and an underlying conductor film becomes insufficient, thereby causing these films to be short-circuited. Note, in particular, the second full paragraph on page 3 of Applicants' specification.

Against this background, Applicants provide a method wherein both ease-in-etching property of the silicon oxide film, and selectivity ratio of etching the silicon oxide

film relative to a silicon nitride film, can be improved, in, illustratively, the SAC process or HARC process. Applicants have found that the objective of both satisfactory ease-in-etching and selectivity can be achieved, wherein the etching is carried out in such a state that a residence time within an etching chamber is controlled to a specific range where selectivity to the silicon nitride insulating film is improved, and that this control is achieved by establishing a low pressure within the chamber and passing the etching gas at a large flow rate. That is, the oxide film is etched in a relative short time, while establishing conditions including, for example, a low pressure and a great flow rate of an inert gas, together with a specific temperature of the substrate (e.g., semiconductor wafer) being etched, so that a good ease-in-etching property and a high silicon oxide/silicon nitride selectivity ratio can be simultaneously realized.

More particularly, in the SAC process, Applicants have found that when the temperature of the wafer being etched is raised under conditions of a low pressure and great flow rate of the inert gas, for example, a good ease-in-etching property and high selectivity ratio can be realized. Note, in particular, Items (1) and (2) on each of pages 77 and 79 of Applicants' specification.

Applicants have also provided processing, which can be used in, for example, the HARC process, to plasma etch a silicon oxide insulating film through a hard mask as an etching mask, so as to form a hole in the silicon oxide insulating film down to a patterned silicon nitride film in such a manner that an upper surface of a silicon plug extending in the silicon nitride film is exposed.

Yamada, et al, discloses a method and system for processing a substrate in the presence of high purity C_5F_8. According to an embodiment disclosed in Yamada, et al,

a gas mixture is introduced into a hermetic treatment chamber that houses a substrate having an SiO_2 layer above an SiN_x layer. The process etches the SiO_2 layer using a gas mixture that includes at least C_4F_8 and CO until the SiN_x layer is exposed, and subsequently etches the SiO_2 layer using C_5F_8 and at least one of CO and O_2 after the SiN_x layer has been exposed. See, column 4, lines 54 - 61. Note also from column 4, line 62 to column 5, line 5. This patent discloses, in a particular application of the etching process, that a gas mixture of C_5F_8 and CO is used to etch a substrate. The atmospheric pressure within the treatment chamber was selected as 40(mTorr), and the temperatures of the upper electrode (108) and the inner wall surface of the treatment chamber were maintained at 60°C whereas the temperature of the lower electrode (110) was maintained at 40°C, in structure seen in Fig. 1 of this patent.

Initially, note that from Fig. 1 of Yamada, et al, the wafer is very close to the lower electrode, described in Yamada, et al as being at a temperature of 40°C. It is respectfully submitted that taking the teachings of Yamada, et al as a whole, including description of temperature of the lower electrode, this patent would have neither taught nor would have suggested the presently claimed subject matter, including a temperature of the substrate being plasma etched ranging from 60 - 140°C, more particularly, 100 - 130°C.

In reviewing the teachings of Yamada, et al as a whole, this patent does not address a temperature of the substrate during etching; and it is respectfully submitted that this patent would have neither taught nor would have suggested such processing as in the present claims, including temperature of the substrate during etching, and advantages thereof as discussed in the foregoing.

Furthermore, it is respectfully submitted that Yamada, et al does not disclose, nor would have suggested, processing including etching which exposes a silicon plug; or, for example, effect of the etching treatment on the silicon plug, and thus would have neither disclosed nor would have suggested that aspect of the present invention, as in, for example, claims 22 - 40.

On page 4 of the Office Action mailed January 13, 2003, the Examiner notes that Yamada, et al does not disclose the temperature of the substrate being plasma etched, but contends that it would have been obvious to one of ordinary skill in the art to optimize the temperature through routine experimentation in order to produce an expected result. However, as recognized by the Examiner, Yamada, et al teaches a temperature of 40°C at the lower electrode. In addition, this reference does not provide any guidance with respect to temperature of the substrate being a process variable having an effect on the processing. In view thereof, it is respectfully submitted that the teachings of the applied reference provide no guidance for modifying the substrate temperature for optimizing the process.

While the Examiner contends that the temperature of the substrate "is commonly determined by routine experimentation", this contention by the Examiner is respectfully traversed. It is respectfully submitted that substrate temperature may, for example, follow through adjustment of other process variables; in any event, absent Applicants' disclosure of their invention, which of course does not constitute prior art, there is no basis for the Examiner to conclude that the temperature of the substrate is commonly determined by routine experimentation, and that it would have been obvious to optimize the temperature through routine experimentation.

While the Examiner refers to optimizing the temperature "in order to produce an expected result", the Examiner has not indicated a basis for concluding that a result of varying temperature of the substrate would be an "expected" result.

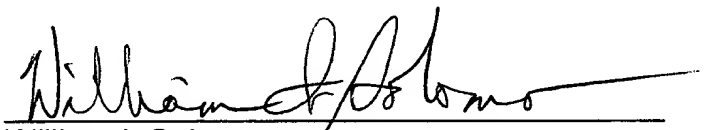
In view of the foregoing comments and amendments, reconsideration and allowance of all claims remaining in the application are respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The changes are shown on the attachment captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 501.40201X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



William I. Solomon
Registration No. 28,565

WIS/jla
(703) 312-6600
Attachment

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon nitride insulating film [on] over a semiconductor substrate;

(b) depositing a silicon oxide insulating film [on] over said silicon nitride insulating film; and

(c) subjecting said semiconductor substrate to a plasma etching treatment using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film,

wherein a residence time of the etching gas within an etching chamber is set at 50 to 700 ms, and

wherein a temperature of said semiconductor substrate being plasma etched ranges from 60 to 140°C.

8. (Amended) A method according to Claim 1, wherein [a] the temperature of said semiconductor substrate being plasma etched ranges from 100 to 130°C.

13. (Amended) A method according to Claim 11, wherein a [the] flow rate of said argon gas ranges from 400 to 800 cm^3/minute.

18. (Amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon nitride insulating film [on] over a semiconductor substrate;

(b) depositing a silicon oxide insulating film [on] over said silicon nitride insulating film; and

(c) subjecting said semiconductor substrate to a plasma etching treatment using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film,

wherein a residence time of the etching gas within an etching chamber is set at 50 to 350 ms, and

wherein a temperature of said semiconductor substrate being plasma etched ranges from 60 to 140°C.

19. (Amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon nitride insulating film [on] over a semiconductor substrate;

(b) depositing a silicon oxide insulating film [on] over said silicon nitride insulating film; and

(c) subjecting said semiconductor substrate to a plasma etching treatment using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film,

wherein a residence time of said etching gas within an etching chamber is set at 100 to 200 ms, and

wherein a temperature of said semiconductor substrate being plasma etched ranges from 60 to 140°C.

20. (Amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon nitride insulating film [on] over a semiconductor substrate;

(b) depositing a silicon oxide insulating film [on] over said silicon nitride insulating film; and

(c) subjecting said silicon oxide insulating film to a plasma etching treatment using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film,

wherein a pressure within an etching chamber during the plasma etching treatment ranges 0.7 to 7 Pa, and a total flow rate of the etching gas passed into said etching chamber is 700 cm^3/minute, and

wherein a temperature of said semiconductor substrate being plasma etched ranges from 60 to 140°C.

21. (Amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon nitride insulating film [on] over a semiconductor substrate;

(b) depositing a silicon oxide insulating film [on] over said silicon nitride insulating film; and

(c) subjecting said silicon oxide insulating film to a plasma etching treatment using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film,

wherein a pressure within said etching chamber during the plasma etching

ranges from 1.3 to 4 Pa, and a total flow rate of said etching gas passed into the etching chamber is at 700 [cm^3/cm] cm^3/minute or over, and

wherein a temperature of said semiconductor substrate being plasma etched ranges from 60 to 140°C.

22. (Amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film [on] over a patterned silicon nitride film with a silicon plug over a semiconductor substrate;

(b) forming a hard mask [on] over said silicon oxide insulating film; and

(c) subjecting said semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the silicon plug is exposed,

wherein a residence time of the etching gas within an etching chamber is set at 50 to 700 ms.

37. (Amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film [on] over a patterned silicon nitride film with a silicon plug over a semiconductor substrate;

(b) forming a hard mask [on] over said silicon oxide film; and

(c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the silicon plug is exposed,

wherein a residence time of the etching gas within an etching chamber is set at 50 to 350 ms.

38. (Amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film [on] over a patterned silicon nitride film with a silicon plug over a semiconductor substrate;

(b) forming a hard mask [on] over said silicon oxide film; and

(c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the silicon plug is exposed,

wherein a residence time of the etching gas within an etching chamber is set at 100 to 200 ms.

39. (Amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film [on] over a patterned silicon nitride film with a silicon plug over a semiconductor substrate;

(b) forming a hard mask [on] over said silicon oxide film; and

(c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the silicon plug is exposed,

wherein a pressure within the etching chamber during the plasma etching ranges from 0.7 to 7 Pa and a total flow rate of the etching gas passed into the etching chamber is 700 cm^3/minute or over.

40. (Amended) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a silicon plug over a semiconductor substrate;

(b) forming a hard mask [on] over said silicon oxide film; and

(c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the silicon plug is exposed,

wherein a pressure within the etching chamber during the plasma etching ranges

from 1.3 to 4 Pa and a total flow rate of the etching gas passed into the etching chamber is 700 cm^3/minute or over.